Docket No.: 42390.P7876X

AMENDMENTS TO THE SPECIFICATION

Please amend the specification on page 1 at line 5 by inserting the following new paragraph and heading:

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of Application No. 09/475,614 filed December 30, 1999, pending.

Please replace the paragraph appearing on page 6, line 10, with the following amended paragraph:

Referring to FIG. 3 2, an exemplary one of the microengines 22a-22f is shown. The microengine 22a includes a control store 70 for storing a microprogram. The microprogram is loadable by the central processor 20. The microengine 70 also includes control logic 72. The control logic 72 includes an instruction decoder 73 and program counter units 72a-72d. The four program counters are maintained in hardware. The microengine 22a also includes context event switching logic 74. The context event switching logic 74 receives messages (e.g., SEQ_#_EVENT_RESONSE; FBI_EVENT_RESPONSE; SRAM_EVENT_RESPONSE; and AMBA_EVENT_RESPONSE) from each one of the share resources, e.g., SRAM 26b, SDRAM 26a, or processor core 20, control and status registers, and so forth. These messages provides information on whether a requested function has completed. Based on whether or not the function requested by a thread has completed and signaled completion, the thread needs to wait for that complete signal, and if the thread is enabled to operate, then the thread is placed on an available thread list (not shown). As earlier mentioned, in one embodiment, the microengine 22a can have a maximum of four threads of execution available.